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10/699,975	11/02/2003	Isaiah O. Oladeji	JESSEN 7-1-4	5032

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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/29/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,975	OLADEJI ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Brief filed August 30, 2006. Claims 6-24 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Specification

1. The disclosure is objected to because of the following informalities: Specification page 1, information and status (abandonment) of parent applications Serial No. 09/966,157 and Serial No. 10/152,305 should be updated. Appropriate correction is required.

Claim Objection

2. Claims 13,16-17,20,22 are objected to because of the following informalities:

** It is inconsistent since base claim 13 recites "non-metallic barrier layer" while dependent claims 16-17,20 recite a different term of "a barrier mask film". Claim 16 recites "a passivation mask film" while base claim 13 recites "a passivation layer".

** Claim 17 recites "silicon carbonite" while claim 7 recites "silicon carbide".

** In claim 22, line 2 and last line, "the feature" is unclear of which features, since there are "first feature" and "second feature".

Appropriate correction is required.

****

*** In view of new grounds of rejection, PROSECUTION IS HEREBY REOPENED. A new ground of art rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(a) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(b) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 112

3. Claims 22-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Re claim 22, original specification including page 9, lines 13-22 does not support and teach "...then removing the metallic mask film...after etching the first and second features..., and before depositing the conductive metal in the feature...".

Re further claim 23, nowhere in the original specification supports and teaches "...patterning a first feature having a predetermined width different from a predetermined width of the first feature, and patterning a second feature having a predetermined width, said second feature being aligned with respect to said first feature". As shown in Figures 10-15, pattern of the first feature is the same width as the first feature, and the second feature is not being aligned with respect to the first feature and not the same as the first feature.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 6-19,21,23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Watatani (6,153,511).

Re claim 6, Watatani teaches a method of forming a dual damascene interconnect structure of an integrated circuit device, said interconnect structure having a low-k dielectric material 78/74 deposited over an underlying metal layer 71, comprising the steps of: (a) forming a tri-part mask layer overlaying the low-k dielectric material 74/78 (Figs 5A-6B; col 5, line 55 through col 8); the mask layer 81 including an etching stopper film 80 (any of SiO_2, SiON, SiN and SiON) in combination with the etching stopper metallic film 82 of TiN, wherein the etch stopper film 80 is formed as a stacking film also including an SiO_2 film as a non-metallic barrier film and an SiC film (col 6, lines 18-30; Figs 5A-5G,6A-6B; col 7, lines 43-55) as a passivation layer, wherein the layer 76 is also as a passivation layer formed over the low-k dielectric material 74, wherein the a non-metallic barrier layer is interposed between a passivation layer and a metallic film 82 to create a tri-part mask layer including the passivation mask film over the low-k dielectric material; the non-metallic barrier mask film over the passivation mask film, and a metallic mask film 82 overlaying the barrier mask film; (b) etching a trench within the mask layer, through at least the metallic mask film 82, without penetrating through the passivation layer 80 (Figs 5A-5G,6A-6B; col 6, lines 31-67); and (c) after etching the trench in the mask layer, then etching a via 89/93 through the mask layer within the trench and through the low-k dielectric material 74/78 to the underlying metal layer before transferring the trench to the low-k dielectric material 78/74 (Figs 5D-5G,6A-6B; col 6, line 31 through col 8, line 22).

Re claim 13, Watatani teaches the method of forming an interconnect structure on an integrated circuit device having a low-k dielectric material 74/78 deposited over an underlying metal layer 71, and a mask layer deposited on the low-k dielectric material (Figs 5A-6B; col 5, line 55 through col 8), and the mask layer having a desired etch selectivity with respect to the low-k dielectric material, the method comprising the forming an etching stopper film 80 (any of SiO_2, SiON, SiN and SiON) in combination with the etching stopper metallic film 82 of TiN, wherein the etch stopper film 80 is formed as a stacking film also including an SiO_2 film as a non-metallic barrier film and an SiC film (col 6, lines 18-30; Figs 5A-5G,6A-6B; col 7, lines 43-55) as a passivation layer, and thus the a non-metallic barrier layer interposed between a passivation layer and a metallic film 82 to create a composite mask layer to increase the etch

selectivity of the mask layer with respect to the low-k dielectric layer, wherein the layer 76 is also as a passivation layer formed over the low-k dielectric material 74.

Re claims 14-15,9-10, wherein said metallic film 82 comprises a refractory metal alloy of titanium nitride (col 6, lines 6-30), and thus comprising a refractory metal of titanium. Re claim 16, forming a passivation mask film over the dielectric material 74/78, forming a barrier mask film over the passivation mask film and said metallic film 82 is formed over the barrier mask film, in which the etching stopper film 80 (any of SiO_2, SiON, SiN and SiON) is formed over substrate in combination with the etching stopper metallic film 82 of TiN, wherein the etch stopper film 80 is formed as a stacking film of an SiO_2 film as a non-metallic barrier film and an SiC film (col 6, lines 18-30) as a passivation layer, wherein the layer 76 of SiO_2, SiN, SiC is also a passivation layer formed over the low-k dielectric material 74 (col 5, lines 5-67). Re claims 17,7, wherein the passivation mask film comprises silicon dioxide or silicon carbide (col 6, lines 18-30; col 5, lines 5-6 7). Re claims 18,8, wherein the non-metallic barrier mask film of the etch stopper layer 80 comprises silicon nitride (SiN) (col 6, lines 18-30; Figs 5A-5G,6A-6B; col 7, lines 43-55). Re claim 11, wherein forming a photoresist layer 84 over the metallic mask film 82, patterning a trench feature in the photoresist layer, etching a trench through the metal mask film 82 and the barrier mask film 80 to the passivation mask film 80/76 (Figs 5A-5G; col 6, line 14 through col 7). Re claim 12, wherein forming a photoresist layer 86 over the low-k dielectric material 78/74, and patterning a via feature in the photoresist layer (Figs 5B-5G; col 6, line 31 through col 7). Re claim 19, including the steps of etching a trench 91 within the low-k dielectric material 78/74 to a predetermined depth of the low-k dielectric material, etching a via 89 through the low-k dielectric material to the underlying metal layer of the low-k dielectric material (Figs 5D-6B; col 7, line 4 through col 8, line 43), and depositing a conductive metal 83 within the via and trench (Figs 5H-5I; col 7, lines 30-42).

Re claim 21, Watatani teaches a method for the fabrication of a semiconductor device including a wafer substrate having a dielectric material formed over a metallization layer formed over said wafer substrate, comprising the steps of: (a) forming a mask layer over the dielectric material wherein said-mask layer includes a passivation film, and said mask layer having a known etch selectivity with respect to the dielectric material; (b) forming a non-metallic barrier layer over the passivation film; (c) depositing a metallic mask film over the barrier layer to

increase the etch selectivity of the mask layer by forming a tri-part mask layer overlaying the low-k dielectric material 74/78 (Figs 5A-6B; col 5, line 55 through col 8); the mask layer 81 including an etching stopper film 80 (any of SiO_2, SiON, SiN and SiON) in combination with the etching stopper metallic film 82 of TiN, wherein the etch stopper film 80 is formed as a stacking film also including an SiO_2 film as a non-metallic barrier film and an SiC film (col 6, lines 18-30; Figs 5A-5G,6A-6B; col 7, lines 43-55) as a passivation layer, wherein the layer 76 is also as a passivation layer formed over the low-k dielectric material 74, wherein the a non-metallic barrier layer is interposed between a passivation layer and a metallic film 82 to create a tri-part mask layer including the passivation mask film over the low-k dielectric material; the non-metallic barrier mask film over the passivation mask film, and a metallic mask film 82 overlaying the barrier mask film; (d) patterning a first feature in the mask layer after depositing the metallic mask film 82 (Fig 5A); (e) etching the first feature through the metallic mask film without exposing the underlying dielectric material after patterning the feature in the mask layer (Figs 5B; col 6, lines 14-67); (f) patterning a second feature in the mask layer, said second feature overlapping at least a portion of the first feature (Fig 5B, col 6, lines 42-67; Figs 6A-6B; col 8); (g) etching the second feature in the dielectric material in accordance with the patterned second feature in the mask layer before removing remaining portions of the passivation mask film and the metallic mask film (Figs 5D-5E, col 6, line 42 through col 7, line 30); (h) transferring the first feature from the mask layer to the underlying dielectric material after etching the second feature through the dielectric material to the metallization layer (Figs 5F-5G, col 7, lines 31-63); and (i) depositing a conductive metal 83 in the first feature and in the second feature (Figs 5H-5I).

Re claim 23, wherein said step of patterning includes patterning a first feature having a predetermined width different from a predetermined width of the first feature, and patterning a second feature having a predetermined width, said second feature being aligned with respect to said first feature (Figs 5A-5C,5F,6A-6B; col 6, lines 42 through col 8). Re claim 24, wherein said etching step includes etching the first feature in the mask layer through the metallic mask film 82 and to the passivation mask film before patterning the second feature (Figs 5A-5D), and then etching the second feature 93 a predetermined depth in the dielectric material 74/78, before etching the first feature 91 of the dielectric material to a predetermined depth of the dielectric

material spaced above the predetermined depth of the second feature (Figs 5D-5G;6A-6B; col 6, lines 42 through col 8).

6. Claims 6-19,21,23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Hasegawa et al (6,53,246).

Re claim 6, Hasegawa teaches a method of forming a dual damascene interconnect structure of an integrated circuit device, said interconnect structure having a low-k dielectric material 14/13 deposited over an underlying metal layer 53, comprising the steps of: (a) forming a tri-part mask layer overlaying the low-k dielectric material 14/13 (Figs 3A-4H;5A-8F; col 7, lines 29-35; col 6, line 8 through col 10; Figs 6A-6F; col 13, line 45 through col 15), wherein the tri-part mask layer including: i. a first mask film 15 over the low-k dielectric material 14 (Figs 3B-3C; col 8, line), wherein the first mask film 15 comprises forming a thin passivation mask layer on the low-k dielectric material 14 before forming a non-metallic barrier mask film of silicon oxide film on the thin passivation mask film (col 8, lines 40-63; Fig 3B), wherein a film 41 also as a passivation film is formed over the low-k dielectric layer 13 (Figs 6A-6F; col 13, line 45 through col 15); and forming a second mask film 16 of silicon nitride or a metal including titanium, titanium nitride, tantalum, and tantalum nitride overlaying the barrier mask film (Fig 3B; col 8, line 64 through col 9; and Figs 3F; col 9, lines 58-65); b. etching a trench within the mask layer, through at least the metallic mask film 16, without penetrating through the passivation layer 15,41 (Fig 3C; col 9, lines 4-67; Figs 6C); and c. after etching the trench (Fig 3C) in the mask layer, then etching a via (Figs 3D-3E; col 9, lines 25-57) through the mask layer within the trench and through the low-k dielectric material 14/13 to the underlying metal layer 53 before transferring the trench to the low-k dielectric material 14/13 (Fig 3F,4G,4H; col 9,lines 58-67; Figs 6D-6F).

Re claim 13, Hasegawa teaches the method of forming an interconnect structure on an integrated circuit device having a low-k dielectric material 14/13 deposited over an underlying metal layer 53, and a mask layer deposited on the low-k dielectric material, and the mask layer having a desired etch selectivity with respect to the low-k dielectric material, the method comprising (a) forming a tri-part mask layer overlaying the low-k dielectric material 14/13 (Figs 3A-4H;5A-8F; col 7, lines 29-35; col 6, line 8 through col 10), wherein the tri-part mask layer

including: i. a first mask film 15 over the low-k dielectric material 14 (Figs 3B-3C; col 8, line), wherein the first mask film 15 comprises forming a thin passivation mask layer on the low-k dielectric material 14 before forming a non-metallic barrier mask film of silicon oxide film on the thin passivation mask film (col 8, lines 40-63; Fig 3B); and forming a second mask film 16 of silicon nitride or a metal including titanium, titanium nitride, tantalum, and tantalum nitride overlaying the barrier mask film (Fig 3B; col 8, line 64 through col 9; and Figs 3F; col 9, lines 58-65),, and thus the a non-metallic barrier layer interposed between a passivation layer and a metallic film to create a composite mask layer to increase the etch selectivity of the mask layer with respect to the low-k dielectric layer 14/13.

Re claims 14-15,9-10, wherein said metallic film 16 alternatively comprises a refractory metal or refractory metal alloy including titanium, titanium nitride, tantalum, and tantalum nitride overlaying the barrier mask film (Fig 3B; col 8, line 64 through col 9; and Figs 3F; col 9, lines 58-65). Re claim 16, forming a passivation mask film over the dielectric material 14/13, forming a non-metallic barrier mask film over the passivation mask film and said metallic film 16 formed over the barrier mask film, wherein the tri-part mask layer including: a first mask film 15 over the low-k dielectric material 14/13 (Figs 3B-3C; col 8, line), wherein the first mask film 15 comprises forming a thin passivation mask layer on the low-k dielectric material 14 before forming a non-metallic barrier mask film of silicon oxide film on the thin passivation mask film (col 8, lines 40-63; Fig 3B), wherein a film 41 is also as a passivation film 41 is formed over the low-k dielectric layer 13 (Figs 6A-6F; col 13, line 45 through col 15); and forming a second mask film 16 of silicon nitride or a metal including titanium, titanium nitride overlaying the barrier mask film (Fig 3B; col 8, line 64 through col 9; and Figs 3F; col 9, lines 58-65). Re claims 17,7, wherein the passivation mask film comprises silicon dioxide (col 8, lines 40-63; col 13, lines 60-65). Re claims 18,8, wherein the non-metallic barrier mask film of the etch stopper layer comprises silicon nitride (SiN) (col 19, lines 62-65). Re claim 11, wherein forming a photoresist layer 17 over the metallic mask film 16, patterning a trench feature in the photoresist layer, etching a trench through the metal mask film 16 and the barrier mask film to the passivation mask film 15,41 (Figs 3C-3F, col 9, line 9-65; Figs 6C-6F, col 13, line 60 through col 15). Re claim 12, wherein forming a photoresist layer 22 over the low-k dielectric material 14/13, and patterning a via feature in the photoresist layer (Fig 3D; col 9, lines 25-47; Fig 6D).

Re claim 19, including the steps of etching a trench within the low-k dielectric material 14/13 to a predetermined depth of the low-k dielectric material, etching a via through the low-k dielectric material to the underlying metal layer of the low-k dielectric material (Figs 3D-3F;; col 9, lines 6-65; Figs 6D-3F col 14, line 46 through col 15), and depositing a conductive metal 31/32 within the via and trench (Figs 4G-4H; col 9, line 66 through col 10).

Re claim 21, Hasegawa teaches a method for the fabrication of a semiconductor device including a wafer substrate having a dielectric material formed over a metallization layer formed over said wafer substrate, comprising the steps of: forming a tri-part mask film by (a) forming a mask layer over the dielectric material wherein said-mask layer includes a passivation film, and said mask layer having a known etch selectivity with respect to the dielectric material; (b) forming a non-metallic barrier layer over the passivation film; (c) depositing a metallic mask film over the barrier layer to increase the etch selectivity of the mask layer (Figs 3A-4H;5A-8F; col 7, lines 29-35; col 6, line 8 through col 10; Figs 6C-6F, col 13, line 60 through col 15), wherein the tri-part mask layer including: a first mask film 15 over the low-k dielectric material 14/13 (Figs 3B-3C; col 8, line), wherein the first mask film 15 comprises forming a thin passivation mask layer on the low-k dielectric material 14 before forming a non-metallic barrier mask film of silicon oxide film on the thin passivation mask film (col 8, lines 40-63; Fig 3B), wherein a film 41 is also as a passivation film 41 is formed over the low-k dielectric layer 13 (Figs 6A-6F; col 13, line 45 through col 15); and forming a second mask film 16 of silicon nitride or a metal including titanium, titanium nitride, tantalum, and tantalum nitride overlaying the barrier mask film (Fig 3B; col 8, line 64 through col 9; and Figs 3F; col 9, lines 58-65); (d) patterning a first feature in the mask layer after depositing the metallic mask film 16 (Fig 3C); (e) etching the first feature through the metallic mask film 16 without exposing the underlying dielectric material after patterning the feature in the mask layer (Fig 3C; col 9, lines 6-24); (f) patterning a second feature in the mask layer, said second feature overlapping at least a portion of the first feature (Fig 3D); (g) etching the second feature in the dielectric material in accordance with the patterned second feature in the mask layer before removing remaining portions of the passivation mask film and the metallic mask film (Figs 3D-3E; col 9, lines 25-57); (h) transferring the first feature from the mask layer to the underlying dielectric material 14/13 after etching the second feature through the dielectric material to the metallization layer

(Fig 3F; col 9, line 58-67); and depositing a conductive metal 32/31 in the first feature and in the second feature (Figs 4G-4H; col 9, line 66 through col 10).

Re claim 23, wherein said step of patterning includes patterning a first feature having a predetermined width different from a predetermined width of the first feature, and patterning a second feature having a predetermined width, said second feature being aligned with respect to said first feature (Figs 3C-3F, col 9, lines 9-67; Fig 6C-6F; col 14, line 46 through col 15) . Re claim 24, wherein said etching step includes etching the first feature in the mask layer through the metallic mask film 16 and to the passivation mask film before patterning the second feature (Figs 3C,6D), and then etching the second feature a predetermined depth in the dielectric material 14/13, before etching the first feature of the dielectric material to a predetermined depth of the dielectric material spaced above the predetermined depth of the second feature (Figs 3C-3F; col 9, lines 9-67;Figs 6C-6F; col 14, line 45 through col 15).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 20,22 are rejected under 35 U.S.C. 102(b) as being anticipated by Watatani (6,153,511) taken with Usami (6,468,8989) and Chan et al (6,312,874).

Watatani teaches a method of forming a dual damascene interconnect structure of an integrated circuit, as applied to claims 6-19,21,23-24 above. Re claims 20,22, Watatani also

teaches depositing the conductive metal 83 on the integrated circuit chip outside of the via and the trench and planarizing the integrated circuit chip (Figs 5H-5I; col 7, lines 30-50) to remove the excess conductive metal.

Re claims 20,22, Watatani already teaches planarizing to remove the excess conductive layer, but lacks removing the metallic mask layer and the barrier mask film down to the passivation film.

However, Usami teaches planarizing to remove the excess conductive layer (Figs 3A-3B; 6A-6B) and removing all of the metallic masking layers 16B down to the top surface of the passivation film (4 in Fig 3A-3B; col 9, lines 15-47; or 24 in Figs 6A-6B, col 11, line 50 through col 12). Chan et al also teaches removing all of the masking layers including the masking layer 56 and the non-metallic barrier film 54 (Figs 3f,3g,3h) down to the top surface of the passivation layer 52 (Fig 3i), before depositing a conductive metal 70 in the first trench feature and a second via feature, as recited in claim 22, (Figs 3i-3j; col 5, line 10 through col 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dual damascene interconnect structure of Watatani by removing the masking layers down to the top surface of the passivating layer, as taught by Usami and Chan. This is because of the desirability to remove the masking layers after etching to form trench and via for the dual damascene interconnect structure so as to form a thin dual damascene interconnect structure.

9. Claims 20,22 are rejected under 35 U.S.C. 102(b) as being anticipated by Hasegawa et al (6,53,246) taken with Usami (6,468,8989) and Chan et al (6,312,874).

Hasegawa teaches a method of forming a dual damascene interconnect structure of an integrated circuit device, as applied to claims 6-19,21,23-24 above. Re claims 20,22, Hasegawa also teaches depositing the conductive metal 31/32 on the integrated circuit chip outside of the via and the trench and planarizing the integrated circuit chip (Figs 4G-4H; col 9, line 66 through col 7) to remove the excess conductive metal, and also to completely remove the metallic mask film 16/21 (col 10, lines 10-35).

Re claims 20,22, Hasegawa already teaches planarizing to remove the excess conductive layer and the metallic mask film, but lacks removing the metallic mask layer and the barrier mask film down to the passivation film.

However, Usami teaches planarizing to remove the excess conductive layer (Figs 3A-3B; 6A-6B) and removing all of the metallic masking layers 16B down to the top surface of the passivation film (4 in Fig 3A-3B; col 9, lines 15-47; or 24 in Figs 6A-6B, col 11, line 50 through col 12). Chan et al also teaches removing all of the masking layers including the masking layer 56 and the non-metallic barrier film 54 (Figs 3f,3g,3h) down to the top surface of the passivation layer 52 (Fig 3i), before depositing a conductive metal 70 in the first trench feature and a second via feature, as recited in claim 22, (Figs 3i-3j; col 5, line 10 through col 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dual damascene interconnect structure of Hasegawa by removing the masking layers to the top surface of the passivating layer, as taught by Usami and Chan. This is because of the desirability to remove the masking layers after etching to form trench and via for the dual damascene interconnect structure so as to form a thin dual damascene interconnect structure.

Response to Arguments

10. Applicant's arguments filed July 14, 2005 have been fully considered and in moot of new ground of rejections.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Oacs-22

Zandra V. Smith
Supervisory Patent Examiner
21 Dec. 2006